In the Claims

Claims 1-46 (canceled)

47. (new) A method of limiting the maximum voltage imposed across switching devices in an RF power amplifier implemented using a complementary metal oxide semiconductor (CMOS), the method comprising:

coupling one or more pairs of switching devices between a voltage differential;

providing an inductance between the switching devices of each respective pair of switching devices; and

operating the RF power amplifier such that the switching devices of any one pair are turned on and off together to drive a load while limiting the maximum voltage imposed across the switching devices.

48. (new) The method of claim 47, wherein first and second pairs of switching devices are coupled between the voltage deferential, wherein the switching devices of the first pair are turned on during a first time period, and the switching devices of the second pair are turned off during the first time period.

49. (new) The method of claim 48, wherein the switching devices of the first pair are turned off during a second time period, and the switching devices of the second pair are turned on during the second time period.

50. (new) The method of claim 48, wherein the load is alternately driven by the first and second pairs of switching devices.

51. (new) The method of claim 47, further comprising driving the one or more pairs of switching devices by repeatedly turning the switching devices of each respective pair on and off.

52. (new) A method of limiting the maximum voltage imposed across switching devices in an RF power amplifier implemented using a complementary metal oxide semiconductor (CMOS), the method comprising:

coupling first and second switching devices between a voltage differential;

providing an inductance between the first and second switching devices; and

operating the first and second switching devices such that the first and second switching devices are turned on and off together to drive a load while limiting the maximum voltage imposed across the switching devices.

53. (new) The method of claim 52, further comprising coupling third and fourth switching devices between a voltage differential, wherein there is an inductance between the third and fourth switching devices.

54. (new) The method of claim 52, wherein the first and second switching devices are turned on during a first time period and the third and fourth switching devices are turned off during the first time period.

55. (new) The method of claim 54, wherein the first and second switching devices are turned off during a second time period and the third and fourth switching devices are turned on during the second time period.

56. (new) The method of claim 54, wherein the load is alternately driven by the first and second switching devices and the third and fourth switching devices.

57. (new) A method of amplifying RF signals in a wireless device, the method comprising:
providing a first switching device having first and second terminals;
providing a second switching device having first and second terminals, wherein the first and second switching devices are implemented using a complementary metal oxide semiconductor (CMOS);
providing an inductance coupled between the second terminals of the first and second switching devices; and
providing a voltage differential between the first terminals of the first and second switching devices.

58. (new) The method of claim 57, wherein the first and second switching devices are driven by signals that repeatedly turn the devices on and off.

59. (new) The method of claim 57, further comprising coupling third and fourth switching devices between a voltage differential, wherein there is an inductance between the third and fourth switching devices.

60. (new) The method of claim 57, wherein the first and second switching devices are turned on during a first time period and the third and fourth switching devices are turned off during the first time period.

61. (new) The method of claim 60, wherein the first and second switching devices are turned off during a second time period and the third and fourth switching devices are turned on during the second time period.

62. (new) The method of claim 60, wherein the load is alternately driven by the first and second switching devices and the third and fourth switching devices.

63. (new) A method of reducing the peak output voltage of an RF amplifier comprising:

providing an inductor having first and second terminals;

providing a first switching device coupled to the first terminal of the inductor and to a first supply voltage;

providing a second switching device coupled to the second terminal of the inductor and to a second supply voltage;

applying a voltage between the first and second terminals of the inductor during a first time period by turning on the first and second switching devices; and

turning off the first and second switching devices during a second time period.

64. (new) The method of claim 63, further comprising providing a first capacitance coupled to the first terminal, providing a second capacitance coupled to the second terminal, wherein current from the inductor charges or discharges the first and second capacitances during the second time period.

65. (new) The method of claim 63, further comprising coupling a load to the first node.

66. (new) The method of claim 63, wherein the load includes a reactive network.

67. (new) The method of claim 63, wherein one of the first and second switching devices is comprised of an n-channel device, and the other of the first and second switching devices is comprised of a p-channel device.

68. (new) The method of claim 63, further comprising differentially coupling a load to the first and second nodes.

69. (new) The method of claim 63, wherein the first and second switching devices are implemented using a complementary metal oxide semiconductor (CMOS).

70. (new) A method of amplifying signals for a wireless RF communication system comprising:

providing a complementary metal oxide semiconductor (CMOS);

providing an inductor having first and second terminals;

forming a first transistor on the complementary metal oxide semiconductor with the first transistor coupled to the first terminal of the inductor and to a first voltage supply;

forming a second transistor on the complementary metal oxide semiconductor with the second transistor coupled to the second terminal of the inductor and to a second voltage supply;

during a first time period, turning on the first and second transistors to apply a voltage between the first and second terminals of the inductor; and

during a second time period, turning off the first and second transistors.

71. (new) The method of claim 70, further comprising providing a third transistor coupled to the first voltage supply and a fourth transistor coupled to the second voltage supply, wherein there is an inductance between the third and fourth transistors.

72. (new) The method of claim 71, further comprising:
during the first time period, turning off the third and fourth transistors; and
during the second time period, turning on the third and fourth transistors.

73. (new) The method of claim 72, wherein the third and fourth transistors are not turned on during the first time period.

74. (new) The method of claim 72, wherein the first and second transistors are not turned on during the second time period.

75. (new) The method of claim 72, further comprising driving the first and second transistors by repeatedly turning the first and second transistors on and off.

76. (new) The method of claim 75, further comprising driving the third and fourth transistors by repeatedly turning the third and fourth transistors on and off.

77. (new) The method of claim 76, further comprising driving the first and second transistors out of phase with the third and fourth transistors.

78. (new) The method of claim 72, further comprising driving a load using current flowing through the first and second transistors during the first time period and using current flowing through the third and fourth transistors during the second time period.

79. (new) The method of claim 70, wherein the first transistors is comprised of an n-channel device, and the second transistor is comprised of a p-channel device.

80. (new) The method of claim 70, wherein the first transistors is comprised of a p-channel device, and the second transistor is comprised of an n-channel device.